CLAIM AMENDMENTS:

Please amend Claim 13 as shown.

1-12. (Canceled)

13. (Currently Amended) A method of making a trench DMOS transistor having overvoltage protection, said method comprising the steps of comprising:

providing a substrate of a first conductivity type;

~~depositing~~ forming a body region by an implantation of a second conductivity type on the substrate ~~said body region having a second conductivity type~~;

forming at least one trench extending through the body region, wherein said body region is formed prior to the step of forming at least one trench ~~and the substrate~~;

depositing an insulating layer that lines the trench and overlies said body region;

depositing a conductive electrode in the trench overlying the insulating layer;

implanting a dopant of the first conductivity type to form a source region in the body region adjacent to the trench;

depositing an undoped polysilicon layer overlying a portion of the insulating layer; and

implanting a dopant of the first conductivity type to form a plurality of cathode regions in the undoped polysilicon layer, said plurality of cathode regions being separated by at least one anode region.

14. (Original) The method of claim 13 wherein the implanting steps forming a source region and a plurality of cathode regions are performed simultaneously.

15. (Original) The method of claim 13 further comprising the step of defining a photolithographic mask over the body region and the undoped polysilicon layer.

16. (Previously Presented) The method of claim 13 wherein the step of depositing an undoped polysilicon layer is performed before the implanting step.

17. (Previously Presented) The method of claim 13 further comprising the step of etching the conductive electrode to expose a portion of the insulating layer overlying the body region.

18. (Previously Presented) The method of claim 13 further comprising the step of etching away a portion of the undoped polysilicon layer overlying the body region and said at least one trench.

19. (Previously Presented) The method of claim 13 wherein said insulating layer is an oxide layer.

20. (Previously Presented) The method of claim 13 wherein said conductive electrode is polysilicon.

21. (Previously Presented) The method of claim 13 further comprising the step of forming a drain electrode on a bottom surface of the substrate.

22. (Original) The method of claim 21 further comprising the step of forming a source electrode coupled to the source region.

23. (Original) The method of claim 19 wherein said oxide layer has a thickness between about 500 and 800 angstroms.

24. (Original) The method of claim 23 wherein said conductive electrode comprises a second layer of undoped polysilicon and a layer of doped polysilicon disposed over said second undoped polysilicon layer.

25. (Original) The method of claim 13 wherein further comprising the step of implanting boron into at least said plurality of cathode regions and said anode to achieve a prescribed diode breakdown voltage.